CANH-TRUNG NGUYEN

FPGA Developer

+84-977-187-626 @ nguyencanhtrung@me.com

Hanoi, Vietnam Date of birth 30 Dec 1990 Place of birth Vietnam

EXPERIENCE

Field Application Engineer

Avnet, Inc.

Jan 2022 – June 2021 Hanoi, Vietnam

Demand creation and providing technical support to customer in South-East Asia, focusing on AMD-Xilinx product lines

- Design and prototype AI vision application on Kria platform including Face Detection/ Recognition and ANPR.
- Providing technical support and training to customers.

ISP implementation

Techvico Company Limited

May 2021 – December 2021 Hanoi, Vietnam

Co-operating with Pinnacle ISP (USA) for designing and prototyping ISP accelerators

- Implementing novel image processing algorithms on FPGA using High Level Synthesis flow.
- Building and prototyping a video streaming system which uses Techvico's accelerators and Xilinx DPU as overlay.

5G-NR RRU

Vinsmart, Vingroup

May 2020 – May 2021 Hanoi, Vietnam

5G-RRU

- Developed 2 RRU vesions based on ADRV9025 and ADRV9009 platform.
- Completed Macrocell 8T8R with peak throughput 800 Mbps

5G-L1

- Lead a team of 3 engineers to develop PDSCH bit-processing (@300MHz). Total processing latency < 150 us (TBS max = 1.2 Megabits)

5G-NR gNodeB

Viettel High Technology Industries Corporation

Dec 2017 – April 2020 Hanoi, Vietnam

5G-L1

Lead a team of 5 engineers to design and implement L1 data channel PUSCH and control channel (PUCCH format 3) on Xilinx FPGA

Radio design

Completed DFE implementation for 2T2R (support DPD, CFR, DUC operations - ACLR = 50 dbm, satisfying 3GPP requirement)

SKILLS

VHDL

MATLAB

C++, C

EDA (Vitis, Vivado, HLS)

Git Petalinux Catapult

PROJECTS

PoC 5G testbed, 2022
5G solution, Quartus and Catapult

PCIe with Intel's MCDMA, 2022
5G solution, Quartus

Smartcam plus, 2022
AI solution, Vitis HLS

Disparity calculation, 2021
ISP accelerators, Vitis HLS

Defect pixels detection and correction, 2021
ISP accelerators, Vitis HLS

Image transformation, 2021
ISP accelerators, Vitis HLS

5G Macrocell 8T8R, 2020, 2021
5G solution, VHDL

PDSCH bit-processing, 2020
be able to run up to 300MHz, VHDL

PUSCH bit-processing, 2019
be able to run up to 250MHz, VHDL

5G NR Digital front-end compatiable with ADI AD9371, AD9375, ADRV9009, 2018
5G solution, VHDL

FINTECH

Microelectronics systems design research group, TU Kaiserslautern

Aug 2016 – Feb 2017 Kaiserslautern, Germany

Designed and prototyped an FPGA-based accelerator for computing intraday financial correlation (the most time-consuming part of Risk Assesment process). Achieved a throughput of 1.087 cycle/floating point number and a 68x speedup in runtime (FPGA@100MHz)

EDUCATION

M.S. in Electrical and Computer Engineering

Technische Universität Kaiserslautern

Oct 2014 – Feb 2017 Kaiserslautern, Germany

- Specilization: Embedded System
- Grade: 1.5 (∼ 92%)

B.Eng. in Electrical and Electronics Engineering

Hanoi University of Science and Technology

Aug 2008 – Jul 2013 Hanoi, Vietnam

- Specilization: Microelectronics
- Grade: 8.64 out of 10

LANGUAGES

Vietnamese	*Native*
English	*Fluent*